AXIe Consortium Approves the new AXIe-2 Software Specification

Submitted from the AXIe Consortium

The AXIe Board of Directors approved a new revision of AXIe-2 Base Software Specification. It, along with all other AXIe specifications, can be found on the specification page here.

The core AXIe specification is AXIe-1, and describes the hardware aspects of the AXIe standard, such as module size, backplane definition, and power and cooling. AXIe-2 adds software requirements for an AXIe chassis or module. AXIe-1 was upgraded last year with revision 3.0. The highlight of that change was to quadruple the PCIe (PCI Express) bus width from four lanes to 16 lanes. This is the widest PCIe fabric of any modular instrument standard, and contributes directly to bus speed. You can read about the upgraded speed here.

While AXIe-2 specifies the software necessary to support AXIe chassis, system modules, and instrument modules, another key goal has been interoperability with PXI systems. Complying with AXIe-2 causes the AXIe products to appear as PXI products, facilitation integration of the two architectures together.

The increase of bus width in AXIe-1 caused the AXIe Consortium Technical Committee to update AXIe-2 to support this new capability. Since the bus width exceeds that of the PXI architecture, new APIs were added that didn't previously exist in the PXI software standards. Since these new capabilities had yet to be tested, the Consortium chose to name the new revision as P2.0, short for Provisional Revision 2.0. This naming is common within other standard bodies, such as the IEEE. Once multiple vendors have implemented and proven the new capabilities, the provisional nature of the specification will be removed, and the standard will simply be AXIe-2 Revision 2.0.

Combined, the latest AXIe-1 and AXIe-2 standards enable unprecedented bus bandwidth of nearly 16GB/sec to or from any slot, supporting next generation mil/aero and wireless communication applications.